REMARKS

Status of the Claims

Claims 1-36 are pending. Claim 1 is rejected. Claims 2-36 are objected to as being dependent upon a rejected base claim.

Claim 1-2, 6, 10, 13-14, 18, 20-21 and 35 have been amended to correct informalities in the claim language and more clearly define the claimed subject matter. Claims 3, 7, 25, 26 and 30-33 have been cancelled. Claims 37-50 have been added to recite subject matter disclosed in the original specification that was not previously claimed. It is noted that Claims 37, 38, 39, 40, 41 and 47 correspond to the original claims 2, 6, 10, 18, 21 and 25, respectively. It is also noted that Claims 42, 43, 44, 45, 46 and 48-50 correspond to the cancelled claim 3, 7, 25, 26, 30 and 31-33, respectively.

Rejection under 35 U.S.C. § 102

In the Office Action dated April 13, 2007, the Examiner rejected Claim 1 as being anticipated by Ooi (USP 5,043,878), Yamaguchi et al. (USP 4,947,373), Dolkas et al. (USP 5,007,051) or Taniai et al. (USP 5,043,935). Applicant respectfully traverses these rejections for at least the following reasons.

Ooi

The Examiner asserts that Ooi discloses first and second information holding circuits (elements 413 and 414 of Fig. 4 of Ooi) formed in a memory cell array for holding information. It is, however, submitted that the elements 413 and 414 are not **formed in a memory cell array**.

- 15 -

Nothing in Ooi teaches or suggests that the elements 413 and 414 are formed in a memory cell array.

The Examiner also asserts that Ooi discloses a first port section (element 437 in Fig. 4 of Ooi) and a second port section (element 438 in Fig. 5 of Ooi) for inputting or outputting information. It is submitted that both elements 437 and 438 are WRITE strobes, which are not for inputting or outputting information.

The Examiner further asserts that Ooi discloses an interchange circuit receiving an interchange control signal and interchanging information held in the first information holding circuit and information held in the second information holding circuit with each other. It is respectfully submitted that the portion of Ooi cited by the Examiner (col. 4, lines 55-60) merely discloses a function of the comparator 124 where the comparator **compares** the content of the level register 122 with the content of the execution level register 123. The comparator 124 does not **interchange** information held in the first information holding circuit and information held in the second information holding circuit with each other.

Therefore, Ooi fails to disclose at least above mentioned limitations recited in Claim 1.

Yamaguchi et al.

The Examiner asserts that Yamaguchi et al. disclose an interchange circuit receiving an interchange control signal and interchanging information held in the first information holding circuit and information held in the second information holding circuit with each other. It is respectfully submitted that the transfer means of Yamaguchi et al. merely **transfers** information of the first or second memory cell group to the first or second serial output register. Assuming the first register or second register shown in Fig. 1 of Yamaguchi et al. were the first and second

- 16 -

information holding circuit, the transfer means would not manipulate the information held in the registers. Thus, the transfer means in Yamaguchi et al. does not **interchange** information held in the first information holding circuit and information held in the second information holding circuit with each other.

Therefore, Yamaguchi et al. fail to disclose at least above mentioned limitations recited in Claim 1.

Dolkas et al.

The Examiner asserts that information holding means shown in the abstract of Dolkas et al. corresponds to first and second information holding circuits of the present invention. It is, however, submitted that the abstract of Dolkas et al. fail to disclose that there are two separate information holding circuits. Further, although the abstract appears to show that the information holding means is coupled to first porting means and second porting means, it fails to disclose a configuration where a first port section is connected to the first information holding circuit and a second port section is connected to the second information holding circuit, respectively.

Further, the Examiner asserts that the element 131 in Fig. 4 of Dulkas et al. corresponds to an interchanging circuit of the present invention. Applicant respectfully submits that the element 131 comprises a microcode and only sets a signal indicating that the buffer is available (see col. 10, line 54 – col. 11 line 2 of Dulkas et al.). Thus, the element 131 is not an interchange circuit for interchanging information held in the first information holding circuit and information held in the second information holding circuit with each other.

In addition, since the abstract states "a method and device for controlling the transmission across a data link," Dulkas et al. fail to disclose an interchanging circuit for interchanging

- 17 -

information held in the first information holding circuit and information held in the second information holding circuit with each other.

Therefore, Dulkas et al. fail to disclose at least above mentioned limitations recited in Claim 1.

Taniai et al.

The Examiner asserts that the transfer request control unit 62 in Fig. 9 of Taniai et al. corresponds to the interchange circuit of the present invention. However, as described in col. 9, lines 13-16 of Taniai et al., the transfer request control unit 62 performs an arbitration of external and internal request.

The Examiner further asserts that col. 1, line 60 – col. 2 line 28 describes interchanging information held in the first information holding circuit and information held in the second information circuit. However, the circuit disclosed in Taniai et al. swaps data stored in a memory cell. In this regard, the Examiner's attention is respectfully directed to Figs. 5A-5C, and col. 4, line 23 – col. 5, line 32 of Taniai et al. According to Taniai et al., the data (B1) stored in a memory is read out to the bus line 1c and temporally stored in the register 4a (Fig. 5A). Then, the data B1 is read out from the register 4a to the bus line 1d and stored in the memory (Fig. 5C). In other words, the circuit of Taniai et al. swaps the data in the memory, but does not swap the data stored in the registers. Thus, the circuit of Taniai et al. does not interchange information held in the first information holding circuit and information held in the second information holding circuit with each other.

Therefore, Taniai et al. fail to disclose at least above mentioned limitations recited in Claim 1.

Anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). At a minimum, the cited prior art does not disclose expressly or inherently the above recited limitation. Thus, Applicant respectfully requests that the Examiner withdraw the rejection of Claim 1.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

Respectfully submitted,

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